## REMARKS

Claims 1, 2, 4-13, and 15-17 are pending. Claims 3 and 14 were previously cancelled. No new matter has been added.

## 35 U.S.C. 102(b) Rejections

Claims 1, 2, 4-13, and 15-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Barnett, U.S. Patent No. 6,173,419 B1.

The Examiner is respectfully directed to independent Claim 1, which recites that an embodiment of the present invention is directed to:

> A method of obtaining debug information, comprising:
> executing a sequence of instructions by a device under test (DUT), wherein said DUT comprises a data line and a clock line;
> executing the sequence of instructions by an emulator device emulating the functions of the DUT and executing the sequence of instructions in lock-step fashion with the DUT;
> the DUT conveying I/O read information to the emulator device over said data line during a data transfer phase; and
> a host computer system reading real-time state and debug information from the emulator device without interrupting the DUT.

Claims 9 and 16 recite similar limitations. Claims 2 and 4-8 are dependent upon Claim 1, and recite further features of the claimed invention. Claims 10-13 and 15 are dependent upon Claim 9, and recite further features of the claimed invention. Claim 17 is dependent upon Claim 16, and recites further features of the claimed invention.

The rejection suggests that Barnett discloses every element of the embodiment of the present invention recited in Claim 1. Applicant respectfully disagrees. Applicant contends that Barnett fails to describe executing a sequence of instructions by a device

under test (DUT), as claimed. Applicant further contends that Barnett fails to describe an emulator device emulating the functions of the DUT and executing the sequence of instructions in lock-step fashion with the DUT, as claimed. Applicant also contends that Barnett fails to describe the DUT conveying I/O read information to the emulator device over said data line during a data transfer phase, as claimed.

Applicant understands Barnett to describe an emulator, for debugging software, programmed into an FPGA; see col. 1, ln. 7-12. Applicant acknowledges that Barnett describes emulating a microcontroller in this FPGA for debugging purposes; see col. 5, ln. 31 – col. 6, ln. 32. Applicant also acknowledges that Barnett discusses an actual microcontroller, and more particularly a bondout integrated circuit which incoporates both a microcontroller and monitoring circuitry; see col. 5, ln. 7-30.

However, Barnett does not disclose or suggest utilizing both the FPGA and the microcontroller being emulated by the FPGA as part of the same system or method for debugging, as claimed. Barnett also fails to discuss executing the same instructions in lockstep on both the microcontroller and the FPGA, as claimed. Barnett also fails to describe or suggest conveying I/O read information from the microcontroller to the emulator over a data line, as claimed. As such, Barnett does not anticipate or render obvious the embodiments of the present invention recited in Claims 1, 9, and 16.

Applicant respectfully asserts that the claimed embodiments of the present invention recited in Claims 1, 9, and 16 are in condition for allowance. Accordingly, Claims 2 and 4-8, dependent upon Claim 1, Claims 10-13 and 15, dependent upon Claim 9, and Claim 17, dependent upon Claim 16, overcome the rejection under 35 U.S.C. § 102(e), as they are dependent upon an allowable base claim.

## Conclusion

In light of the above-listed amendments and remarks, Applicants respectfully request allowance of the remaining Claims.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

WAGNER, MURABITO & HAO LLP

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Kevin A. Brown
Reg. No. 56,303
Two North Market Street
Third Floor
San Jose, California 95113
(408) 938-9060